What is claimed is:

1. A semiconductor device comprising:

a field effect transistor including:

a semiconductor layer formed on an insulator;

a gate insulating film formed on said semiconductor layer;

a gate electrode formed on said gate insulating film and extending in a first direction; and

source/drain regions formed in said semiconductor layer on both sides of said gate electrode by heavily introducing a first conductivity type impurity;

a body contact region in which a second conductivity type impurity is heavily introduced into said semiconductor layer;

a partial isolating region in which a field insulating film thicker than said gate insulating film intervenes between said semiconductor layer and an extending portion of said gate electrode, and an impurity with the same conductivity type as said body contact region is introduced into said semiconductor layer; and

a full isolating region in which said semiconductor layer on said insulator is removed,

wherein said full isolating region is formed to

be in contact with at least a part of a side parallel to said first direction of said source/drain regions of said field effect transistor.

2. The semiconductor device according to claim 1, wherein said gate electrode comprises:

a first gate electrode layer having substantially a same thickness as said field insulating film; and

a second gate electrode layer formed on said first gate electrode layer and extending over a carrier path.

3. The semiconductor device according to claim 2, wherein said first gate electrode layer and said second gate electrode layer are made of a material deposited in different processes.

4. The semiconductor device according to claim 3, wherein said first gate electrode layer and said second gate electrode layer are made of different materials.

5. The semiconductor device according to claim 1, wherein an impurity density in said semiconductor layer in a part of said partial isolating region contiguous to a device region in which said field effect transistor is provided is lower than an

impurity density in said semiconductor layer in the other part of said partial isolating region.

6. The semiconductor device according to claim 1, wherein an impurity density in said semiconductor layer in a part of said partial isolating region contiguous to a device region in which said field effect transistor is provided is lower than an impurity density in said semiconductor layer in the other part of said partial isolating region and is the same as an impurity density in said semiconductor layer in said device region.

7. The semiconductor device according to claim 2, wherein an impurity density in said semiconductor layer in a part of said partial isolating region contiguous to a device region in which said field effect transistor is provided is lower than an impurity density in said semiconductor layer in the other part of said partial isolating region and is the same as an impurity density in said semiconductor layer in said device region.

8. The semiconductor device according to claim 1, wherein said full isolating region is formed to be in contact with the whole sides parallel to said first direction of said source/drain regions of said field

effect transistor.

9. The semiconductor device according to claim 1, wherein said full isolating region is formed to be in contact with the whole sides parallel to said first direction of said source/drain regions of said field effect transistor and a part of a side perpendicular to said first direction of said source/drain regions.

10. The semiconductor device according to claim 1, wherein only said full isolating region is provided between adjacent said field effect transistors.

11. The semiconductor device according to claim 1, wherein said full isolating region is formed to be in contact with a part of a side parallel to said first direction of said source/drain regions of said field effect transistor and the whole of one side perpendicular to said first direction of said source/drain regions.

12. The semiconductor device according to claim 1, wherein a plurality of said field effect transistors are provided in one block surrounded by said full isolating region.

13. The semiconductor device according to claim 1,

wherein a p-channel type said field effect transistor and a n-channel type said field effect transistor are provided in different blocks surrounded by said full isolating region, respectively.

14. The semiconductor device according to claim 1, wherein a plurality of p-channel type said field effect transistors and a plurality of n-channel type said field effect transistors are provided in different blocks surrounded by said full isolating region, respectively.

15. The semiconductor device according to claim 1, wherein said full isolating region defining a block including a plurality of said field effect transistors is formed to be in contact with a side of said source/drain regions.

16. The semiconductor device according to claim 1, wherein said full isolating region defining a block including one said field effect transistor is formed to be in contact with a side of said source/drain regions.

17. A method for manufacturing a semiconductor device comprising:

(a) forming a CMP (Chemical Mechanical Polishing)

mask to cover a device region and a body contact region on a semiconductor layer on an insulator, said CMP mask being composed of an upper mask layer resistant to a CMP and a lower mask layer made of a conductive material or a material which is made conductive by introducing impurity;

(b) introducing a second conductivity type impurity into at least a portion of said semiconductor layer which is not covered by said CMP mask, said second conductivity type impurity is different from an impurity which is to be introduced into source/drain regions;

(c) forming a full isolating region by removing said semiconductor layer on said insulator in a part of a region contiguous to said CMP mask;

(d) forming wholly a second insulating film different from a material of said CMP mask and planarizing said second insulating film by a CMP;

(e) removing said upper mask layer of said CMP mask and forming an upper gate electrode layer made of a conductive material or a material which is made conductive by introducing impurity;

(f) removing said upper gate electrode layer and said lower mask layer of said CMP mask in said body contact region and a part of said device region, to form a gate electrode composed of a residual of said upper gate electrode layer and said lower mask layer

of said CMP mask and extending in a first direction; and

(g) forming source/drain regions in said semiconductor layer on both sides of said gate electrode to form a field effect transistor,

wherein said full isolating region is formed to be in contact with at least a part of a side parallel to said first direction of said source/drain regions of said field effect transistor.

18. The method for manufacturing a semiconductor device according to claim 17, said (d) forming is carried out after said (c) forming.

19. The method for manufacturing a semiconductor device according to claim 17, said (c) forming is carried out after said (d) forming.

20. A method for manufacturing a semiconductor device comprising:

(h) forming a CMP (Chemical Mechanical Polishing) mask to cover a device region and a body contact region on a semiconductor layer on an insulator, said CMP mask being composed of an upper mask layer resistant to a CMP and a lower mask layer made of a conductive material or a material which is made conductive by introducing impurity;

(i) introducing a second conductivity type impurity into at least a portion of said semiconductor layer which is not covered by said CMP mask, said second conductivity type impurity is different from an impurity which is to be introduced into source/drain regions;

(j) forming wholly a second insulating film different from a material of said CMP mask and planarizing said second insulating film by a CMP;

(k) removing said upper mask layer of said CMP mask and forming an upper gate electrode layer made of a conductive material or a material which is made conductive by introducing impurity;

(l) removing said upper gate electrode layer and said lower mask layer of said CMP mask in said body contact region and a part of said device region, to form a gate electrode composed of a residual of said upper gate electrode layer and said lower mask layer of said CMP mask and extending in a first direction;

(m) forming source/drain regions in said semiconductor layer on both sides of said gate electrode to form a field effect transistor;

(n) covering said field effect transistor by an interlayer insulating film and planarizing said interlayer insulating film; and

(o) forming a full isolating region by removing said semiconductor layer in a part of a region

contiguous to said source/drain regions;

wherein said full isolating region is formed to be in contact with at least a part of a side parallel to said first direction of said source/drain regions of said field effect transistor.

21. The method for manufacturing a semiconductor device according to claim 17, wherein said CMP mask is a multiple-layer including a Si_3N_4 film as a top layer.

22. The method for manufacturing a semiconductor device according to claim 17, wherein said CMP mask is a multiple-layer including a SiO_2 film as a top layer and a Si_3N_4 film as a second layer under said top layer.

23. The method for manufacturing a semiconductor device according to claim 17, wherein said CMP mask is a multiple-layer including a Si_3N_4 film as a top layer and a polysilicon film as a second layer under said top layer.

24. The method for manufacturing a semiconductor device according to claim 17, wherein said CMP mask is a multiple-layer including a Si_3N_4 film as a top layer, a SiO_2 film as a second layer under said top

layer, and a polysilicon film as a third layer under said second layer.

25. The method for manufacturing a semiconductor device according to claim 17, wherein said (b) introducing is carried out such that said second conductivity type impurity is the same as an impurity which is to be introduced into said semiconductor layer in said body contact region.

26. The method for manufacturing a semiconductor device according to claim 17, wherein materials of said lower mask layer of said CMP mask and said upper gate electrode layer are polysilicon.

27. The method for manufacturing a semiconductor device according to claim 17, wherein said upper gate electrode layer is a multiple-layer made of a conductive material or a material which is made conductive by introducing impurity.

28. The method for manufacturing a semiconductor device according to claim 17, wherein said lower mask layer of said CMP mask is made of polysilicon and said upper gate electrode layer is made of metal.

29. The method for manufacturing a semiconductor

device according to claim 17, wherein a side wall is formed next to said CMP mask after said (a) forming, and said (b) introducing is carried out such that said second conductivity type impurity is introduced into at least a portion of said semiconductor layer which is not covered by said CMP mask and said side wall.

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30. A semiconductor device which has a transistor, comprising:

a semiconductor layer formed on an insulating film;

an active region formed in said semiconductor layer, said active region including a source region, a drain region and a channel region between said source region and said drain region;

a gate electrode formed over said channel region and extending in a first direction;

a body contact region formed in said semiconductor layer apart from said active region;

a carrier path formed in said semiconductor layer to connect said active region and said body contact region;

a first isolating region formed on said insulating film to be in contact with at least one of a first side of said source region parallel to said first direction and a second side of said drain region parallel to said first direction; and

a second isolating region extending from said first isolating region over said carrier path,

wherein said semiconductor layer in said carrier path has substantially a same thickness as said semiconductor layers in said active region and said body contact region.